REMARKS

Prior to the present amendment and response, claims 1-3, 6-8, 11-15, and 18-20 were pending in the application. Claims 1-3 and 6-8 have been allowed. By the present amendment, claims 11 and 19 have been amended and claim 12 has been canceled. Thus, after the present amendment, claims 1-3, 6-8, 11, 13-15, and 18-20 remain in the present application. Reconsideration and allowance of outstanding claims 11, 13-15, and 18-20 in view of the above amendments and following remarks are respectfully requested.

A. Rejections of Claims 11-15 and 18-20 under 35 USC §102(e)

The Examiner has rejected claims 11-15 and 18-20 under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication Number US 2001/0042190 to Tremblay, et al. ("Tremblay"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 11 and 19, is patentably distinguishable over Tremblay.

As disclosed in the present application, conventional approaches in the processor architecture field do not adequately address the problem of consumption of chip area for wide buses, such as wide "move" buses linking various register file banks. Various embodiments according to the present invention address and overcome the need in the art for speeding up the very long instruction word ("VLIW") processor architecture and reducing power consumption and reducing chip area while accommodating multiple register file banks and multiple execution units.

An exemplary embodiment of the present invention, as shown in Figure 2, includes register file banks 252 and 254. Register file bank 252 comprises read ports 280 and write ports 282, while register file bank 254 comprises read ports 290 and write ports 292. Data path block 212 comprises execution units such as multipliers 216 and 220 and ALUs ("arithmetic logic unit") 218 and 222, while data path block 214 comprises execution units such as multipliers 224 and 230 and ALUs 226 and 228.

As shown in Figure 3, scheduling restrictions are imposed on the relationship between read ports, buses, and execution units included in the present invention. For example, during a single clock cycle, read bus 264 is utilized to transport an operand from read port R0 in register file bank 252 to either multiplier 224 or ALU 226 in data path block 214. See, for example, present application, page 17, lines 16-18. Consequently, the present invention avoids the need for a wider bus that can accommodate concurrent transport of two operands, one to multiplier 224 and another to ALU 226. Therefore, the scheduling restrictions result in area savings since the need for additional ports and wider buses is avoided. Furthermore, since the read buses are narrower and efficiently used during execution of instructions, excess power consumption is eliminated and significant power savings also result.

Tremblay, in contrast, discloses a VLIW processor having a plurality of functional units, such as media functional unit (MFU) 220 and general functional unit (GFU) 222 shown in Figure 2 of Tremblay. In Tremblay, for example, GFU 222 "is a RISC processor capable of executing arithmetic logic unit (ALU) operations, loads and stores,

branches, and various specialized and esoteric functions..." Tremblay, paragraph 36, lines 1-4. As such, the functional units disclosed in Tremblay are merely comparable to the data path blocks disclosed in the present invention, since as discussed above, each data path block in the present invention comprises execution units such as multiplier 216 and ALU 218 (shown in Figure 2 of the present invention).

Tremblay, however, does not impose a scheduling restriction such that "during a single clock cycle an operand residing in one of said first plurality of read ports is used by only one execution unit in said first plurality of execution units in said first data path block and by only one execution unit in said second plurality of execution units in said second data path block," as required by amended independent claim 11. Tremblay discloses maintaining a "scoreboard" that is "used to manage most interlocks between the general functional unit 222 and the media functional units 220" and that "operates by tracking a record of an instruction packet or group from the time the instruction enters a functional unit until the instruction is finished and the result becomes available." Tremblay, paragraph 45, lines 1-3 and paragraph 43, lines 10-13. However, Tremblay fails to teach, disclose, or suggest the use of any scheduling restrictions on the use of an operand by each *execution unit* in a plurality of execution units included in a data path block as provided by the present invention. As a result, the configuration disclosed in Tremblay does not avoid the need for a wider bus that can accommodate concurrent transport of two operands.

Independent claim 19 has been amended to include limitations similar to amended independent claim 11 and now recites "wherein during a single clock cycle an operand residing in one of said respective plurality of read ports is used by only one execution unit in said respective plurality of execution units." Thus, based on the reasons stated above, amended independent claim 19 is also patentably distinguishable over Tremblay.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by amended independent claims 11 and 19 is not taught, disclosed, or suggested by the art of record. As such, the claims depending from amended independent claims 11 and 19 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 11 and 19, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 11, 13-15, and 18-20 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to all claims 1-3, 6-8, 11, 13-15, and 18-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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